REMARKS

I. CLAIM 12 IS NOT ANTICIPATED BY SEIDLER

Claims 3, 8 and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Seidler. Claims 3 and 8 have been canceled, rendering the rejection thereto moot. This rejection is respectfully traversed for the following reasons.

Claim 12 recites in pertinent part "a plurality of semiconductor device units, ***each*** of said semiconductor device units including: a semiconductor chip ... a packaging board for mounting said plurality of semiconductor device units; wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board ..." (emphasis added). The Examiner alleges that substrate 260' reads on the recited "packaging board" of claim 12. However, assuming *arguendo* substrate 260' can be read as a packaging board, it is submitted that Seidler does NOT disclose "a packaging board for mounting said ***plurality*** of semiconductor device units." That is, if the Examiner interprets substrate 260' as a "packaging board", then Figure 8 relied on by the Examiner discloses only ***one*** semiconductor unit 260 mounted on the alleged packaging board 260'. Accordingly, Figure 8 of Seidler does not disclose a ***plurality*** of semiconductor device units, where ***each*** of the units includes the limitations recited in lines 4-11 of claim 12, and where the plurality of semiconductor units are mounted on a packaging board (*see, e.g.*, Figures 14-16 of Applicants' specification showing at least two units 1,7 coupled to a packaging board 10; whereas Seidler discloses only two alleged units without the packaging board or as relied on by the Examiner, one packaging board and one semiconductor unit).

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Seidler does not disclose or suggest, *inter alia*, "a packaging board for mounting said plurality of semiconductor device units", it is submitted that Seidler does not anticipate claim 12.

Claim 12 further recites in pertinent part, a "conductive clip having elasticity for clamping objects." The Examiner alleges that the alleged conductive member 10 of Seidler has "elasticity for clamping objects." However, Seidler appears to be completely silent as to the clip 10 being configured to function as a clamp. The dictionary definition of clamp is as follows:

> a device designed to press two or more parts together so as to hold them firmly (Merriam-Webster's).

It is respectfully submitted that the clip 10 of Seidler does NOT necessarily "press [the opposing contact pads 62 and 64] together so as to hold them firmly." There is nothing in Seidler that suggests clip 10 MUST ***clamp*** the opposing pads 62 and 64 together. Accordingly, Seidler does not anticipate claim 10. As is well known, a proper rejection under § 102 requires the prior art to ***necessarily*** disclose each and every claim limitation.

As defined in the dictionary according to its ordinary meaning, a clamp must be configured to ***affirmatively*** press two elements together rather than simply have an incidental resistive force. That is, a clamp has an intrinsic biasing force for holding two parts ***firmly*** together. In contrast, Seidler does not provide any suggestion that clip 10 is specifically configured to provide a clamping force. Even assuming *arguendo* clip 10 ***could*** be a clamp if bent/configured or interacted with other elements in certain ways, such a possibility does NOT indicate that clip 10 ***is*** a clamp. For example, a paper clip when bent in certain ways will have a

clamping force and when bent in other ways will NOT have a clamping force. Turning to Seidler, there is nothing suggesting that clip 10 is bent/configured to act as a clamp.

Nevertheless, it is submitted that clip 10 of Seidler appears to be configured NOT as a clamp, which is evidenced by the fact that the clip 10 is coupled ***indirectly*** to the pads 62/64 using ***thin*** extensions 18 through elements 50/26. If the Examiner maintains this rejection, it is respectfully requested that the Examiner explain why the alleged clip 10 of Seidler MUST function as a clamp, rather than simply be equivalent to a bent thin metal wire.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Seidler does not disclose or suggest, *inter alia*, a "conductive clip having elasticity for clamping objects" as recited in claim 12, it is submitted that Seidler does not anticipate claim 12.

Based on all the foregoing, it is submitted that claim 12 is patentable over Seidler. Accordingly, it is respectfully requested that the rejection of claim 12 under 35 U.S.C. § 102(b) over Seidler, be withdrawn.

II. CLAIMS 4, 9 AND 13 ARE NOT ANTICIPATED BY TSUBOSAKI ET AL.

Claims 4, 9 and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tsubosaki et al.. This rejection is respectfully traversed for the following reasons.

The Examiner asserts that the alleged conductive member 3 shown in Figure 9 of Tsubosaki et al. is "formed on the ***surface*** of said semiconductor chip." In contrast, as shown in Figure 9, no portion of the alleged conductive member 3 is formed on ***the surface*** of the chip 1. Instead, the alleged conductive member 3 is entirely spaced away from the chip 1 by insulative

adhesives 2,7 and electrode 4. Claims 4, 9 and 13 have been amended to emphasize the distinction between the present invention and Tsubosaki et al.. One of the benefits of the present invention as recited in claims 4, 9 and 13 is the ability to attain a fine pitch pattern.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Tsubosaki et al. does not disclose or suggest, *inter alia*, a "conductive layer formed on the ***surface*** of said semiconductor chip" as recited in each of claims 4, 9 and 13, it is submitted that Tsubosaki et al. does not anticipate claims 4, 9 and 13.

Based on the foregoing, it is submitted that claims 4, 9 and 13 are patentable over Tsubosaki et al.. Accordingly, it is respectfully requested that the rejection of claims 4, 9 and 13 under 35 U.S.C. § 102(b) over Tsubosaki et al., be withdrawn.

III. CLAIM 6 IS NOT ANTICIPATED BY EIDE

Claim 6 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Eide. This rejection is respectfully traversed for the following reasons.

Claim 6 recites in pertinent part, "at least a first electrode ..., at least a second electrode or an insulation layer ...; and at least a conductive member ...; wherein a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrode ... and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns." The Examiner alleges that the claimed first and second electrodes are located under the conductors 10, and the claimed first and second

conducting patterns which extend from the respective electrodes are located under the bumps 5.

However, Eide is completely silent as to what is formed on the TSOP chips 8. Rather, Eide discloses simply a device which converts I/O terminal leads of a TSOP chip 8 into a BGA-type connection so as to enable stacking IC's (*see* col. 3, lines 5-11; other than leads as shown in Figure 1, Eide is completely silent as to the IC elements formed on the chips 8). Apparently, the Examiner is taking the position that somewhere underneath the conductor 10 and bumps 5 there are ***inherently*** electrodes and conducting patterns. It is respectfully submitted, however, that the TSOP chips 8 do NOT necessarily have ***both*** electrodes ***and*** conducting patterns under the conductive elements 5, 10 in the manner recited in claim 6, let alone "a bump [that] is provided between said first conducting pattern and said second conducting pattern, ***which face to each other***, for electrically connecting said two conducting patterns." For example, alleged conductive patterns on the stacked chips of Eide do NOT necessarily have to face each other nor do they have to be connected to each other by the bumps 5. As mentioned above, Eide is directed merely to connecting the edge leads of the chips 8 (*see* Figure 1) to bumps or a BGA using a conductive circuit 5,10, but is completely silent as to the relative arrangement of electrodes and/or conductive patterns on the chips themselves. Accordingly, even assuming *arguendo* there are electrodes under the circuit 10, 5 as alleged by the Examiner, this conclusion does NOT necessitate that there MUST also be conductive patterns extending from the electrodes, let alone patterns which face each other on opposing chips and which are connected via a bump in the manner recited in claim 6.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Eide does not disclose or

suggest the particular arrangements of electrode/conductive patterns on the chip as recited in claim 6, it is submitted that Eide does not anticipate claim 6.

Based on the foregoing, it is submitted that claim 6 is patentable over Eide. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. § 102(e) over Eide, be withdrawn.

IV. CLAIMS 14-15 ARE NOT ANTICIPATED BY CHUNG

Claims 14 and 15 stand rejected under 35 U.S.C. § 102 as being anticipated by Chung. This rejection is respectfully traversed for the following reasons.

Claim 14 recites in pertinent part, "wherein each of said plurality of semiconductor chips has first and second opposing side surfaces arranged adjacent to first and second spacer members of said plurality of spacer members, respectively." In contrast, each of the chips 420 of Chung have opposing side surfaces which are arranged adjacent to the ***same*** spacer member 410 (*see* Figure 19, illustrating a single, continuous layer which is folded around each semiconductor chip so as to surround almost the entire chip, whereas the arrangement of the present invention is capable of surrounding only the side surfaces so to improve spacing). As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because Chung does not disclose each limitation recited in claim 14, it is submitted that Chung does not anticipate claim 14, nor any claim dependent thereon.

Based on the foregoing, it is submitted that claims 14 and 15 are patentable over Chung. Accordingly, it is respectfully requested that the rejection of claims 14 and 15 under 35 U.S.C. § 102(e) over Chung, be withdrawn.

V. CLAIM 16 IS PATENTABLE OVER CHUNG IN VIEW OF MIYOSHI

Claim 16 stands rejected under 35 U.S.C. § 103 over Chung in view of Miyoshi. This rejection is respectfully traversed for the following reasons.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.,*** 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 14 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. Further, it is submitted that the dependent claims are independently patentable by adding novel and non-obvious features to the combination. In particular, it is submitted that the proposed combination is improper.

The semiconductors of Chung are completely surrounded by insulative material so as to preclude the ability to use the alleged supporting members 61 of Miyoshi for connecting the stacked chips. In addition, as the chips of Chung are already connected to each other, there is no disclosed need or desire to connect them in the manner taught by Miyoshi. Accordingly, it is submitted that the proposed combination does not have the requisite motivation from the prior art. Rather, the proposed combination is based solely on improper hindsight reasoning whereby the Examiner selected bits and pieces of the prior art and used only Applicants' specification as a guide to reconstruct the claimed invention.

That is, it is submitted that the proposed combination is improper because the Examiner has not provided the requisite ***objective*** evidence ***from the prior art*** that "suggests the desirability" of the proposed combination. As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the

proposed combination using ***objective*** evidence. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that Chung can be modified by Miyoshi, it is submitted that the "mere fact that [Chung and Miyoshi] can be combined ... does not render the resultant combination obvious" because nowhere does the ***prior art*** "suggest the desirability of the combination" as set forth by the Examiner. The Examiner is further directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were ***individually*** known in the art is ***not*** sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that Chung and Miyoshi "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no ***objective*** reason on the record to combine the teachings of the cited prior art. In contrast, Chung and Miyoshi are completely silent as to suggesting the ***combination*** of providing a stacked semiconductor with supporting members.

At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that

the ***combination*** of elements recited in the claims is known or suggested in the art. For all the foregoing reasons, it is submitted that the proposed combination of Chung and Miyoshi is improper.

Based on all the foregoing, it is submitted that claim 16 is patentable over Chung in view of Miyoshi. Accordingly, it is respectfully requested that the rejection of claim 16 under 35 USC 103, be withdrawn.

VI. NEW CLAIMS

Claims 17-19 are submitted to be allowable based on their own merits, in addition to being dependent on novel claims 3, 8 and 12, respectively. In particular, Seidler does not disclose "wherein said conductive member includes a first conductive end which contacts said first electrode, and a second conductive end which contacts said second electrode or said insulation layer." In contrast, the alleged electrode 62,262 is contacted by a NON-conductive element 50,250, respectively.

VII. CONCLUSION

Having fully and completely responded to the Office Action, Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

David M. Spencer for

Stephen A. Becker
Registration No. 26,527 (Reg. # 48,562)

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 SAB:MWE
Facsimile: (202)756-8087
Date: February 19, 2003

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APPENDIX

4. (Twice Amended) A semiconductor device comprising:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip,

wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

6. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked on each other,

wherein a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second [electrodes] electrode or insulation layer, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns.

9. (Thrice Amended) A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked on each other, and said conductive members are connected to each other,

wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

13. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

a packaging board for mounting said plurality of semiconductor device units;

wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board,

wherein each of said conductive members is comprised of conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

14. (Twice Amended) A semiconductor device comprising:

a plurality of semiconductor chips each having electrodes formed on the major surface thereof, and

a plurality of spacer members each having a conductive pattern on the surface thereof,

wherein each of said plurality of semiconductor chips has first and second opposing side surfaces arranged adjacent to first and second spacer members of said plurality of spacer members, respectively;

wherein said semiconductor chips and said spacer members are stacked alternately such that said electrodes of said semiconductor chips directly contact corresponding conductive patterns at a portion of the corresponding conductive patterns formed on the surface of the spacer member and are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other.